IN THE CLAIMS

Please amend claims 1 - 3, 7, 9, 11, 13 - 15, 17, and 19 and add new claim 23 to read as follows:

1. (Amended) A semiconductor apparatus comprising:

a semiconductor device to be mounted on a circuit board;

a plurality of conductive posts electrically connected to the semiconductor device; and

[a plurality of conductive bumps each provided on an outer end of each of the conductive posts, so that the plurality of conductive bump is soldered onto the circuit board when the semiconductor device is mounted on the circuit board, wherein

a distance between a peripheral edge of the semiconductor device and an outer edge of the conductive post is determined to be narrow so that a solderbility or wetting condition of the conductive bumps can be visibly recognized easily] means for mounting the device onto a circuit board by soldering, including a plurality of conductive bumps respectively positioned on an outer end of each of the conductive posts for soldering onto the circuit board, wherein a peripheral edge of a resin covering for sealing a surface of the semiconductor device and an outer edge of the conductive post are separated by a distance narrower than a height of the conductive post.

2. (Amended) A semiconductor apparatus according to claim 1, wherein the distance is in a range between 50 [to] and 100 micrometers.

3. (Amended) A semiconductor apparatus according to claim 1, wherein the semiconductor device is provided with a plurality of electrode pads connected to the conductive posts, the electrode pads being arranged on a line extending [the] in a center portion of the semiconductor device.

4. A semiconductor apparatus according to claim 1, wherein the semiconductor device is provided with a plurality of electrode pads connected to the conductive posts, each of the electrode pads being arranged between two adjacent conductive posts.

5. A semiconductor apparatus according to claim 1, wherein the semiconductor device is provided with a plurality of electrode pads connected to the conductive posts, each of the electrode pads being arranged directly under a corresponding conductive post.

6. A semiconductor apparatus according to claim 1, wherein the conductive bumps are of solder.

7. (Amended) A semiconductor apparatus comprising:

a semiconductor device [to be mounted on a circuit board];

a plurality of conductive posts electrically connected to the semiconductor device;

[a plurality of conductive bumps each provided on an outer end of each of the conductive posts, so that the plurality of conductive bumps are soldered onto the circuit board when the semiconductor device is mounted on the circuit board] means for mounting the device onto a circuit board by soldering, including a plurality of conductive bumps respectively positioned on an outer end of each of the conductive posts for soldering onto the circuit board; and

a molding resin [which covers] covering a surface of the semiconductor device, wherein the molding resin is shaped to have a step along the entirety of a peripheral edge of the semiconductor device [entirely], the step having upper and lower level portions.

8. A semiconductor apparatus according to claim 7, wherein the difference in level between the upper portion and lower portion of the step is half of a thickness of the mold resin.

9. (Amended) A semiconductor apparatus according to claim 7, wherein the difference in level between the upper portion and lower portion of the step is in a range between 40 [to] and 60 micrometers.

10. A semiconductor apparatus according to claim 7, wherein the conductive bumps are of solder.

11. (Amended) A semiconductor apparatus comprising:

a semiconductor device [to be mounted on a circuit board];

a plurality of conductive posts electrically connected to the semiconductor device;

[a plurality of first conductive bumps each provided on an outer end of each of the conductive posts, so that the plurality of first conductive bumps are soldered onto the circuit board when the semiconductor device is mounted on the circuit board];

means for mounting the device onto a circuit board by soldering, including a plurality of first conductive bumps respectively positioned on an outer end of each of the conductive posts for soldering onto the circuit board;

a molding resin [which covers] covering a surface of the semiconductor device without covering a peripheral side surface of [each] of the [semiconductor device] conductive posts; and

an insulating layer [which is] formed [at portions corresponding to the conductive posts and at a] on a peripheral [portion] surface of the semiconductor device[, wherein and] between an upper surface of the semiconductor device and the conductive posts, wherein the molding resin is shaped to have a peripheral side

surface on the identical plane with the peripheral side surface of the semiconductor device.

12. A semiconductor apparatus according to claim 11, wherein the insulating layer is formed to have a width of 100 to 200μm.

13. (Amended) A semiconductor apparatus according to claim 11, further comprising

a plurality of second conductive bumps each provided on a respective [the] peripheral side surface of [the] a respective one of the conductive posts.

14. (Amended) A semiconductor apparatus according to claim 11, wherein the first conductive bumps are of solder.

15. (Amended) A method for fabricating a semiconductor apparatus according to claim 7, comprising the steps of:

providing a semiconductor wafer on which a plurality of semiconductor devices are formed, each of the semiconductor device having electrode pads thereon;

providing a plurality of conductive post connected to the electrode pads of the semiconductor devices;

molding the semiconductor devices with a molding resin so that an upper surface of the molding resin is on the same plane with upper surfaces of the conductive posts;

removing a part of the molding resin to be located at a peripheral edge so that the peripheral edge of the molding resin has a step, the step having upper and lower level portions;

providing conductive bumps on outer ends of the conductive posts; and

dicing the semiconductor wafer to form a plurality of individual semiconductor [apparatus] apparatuses.

16. A method according to claim 15, wherein the difference in level between the upper portion and lower portion of the step is half of a thickness of the mold resin.

17. (Amended) A method according to claim 15, wherein the difference in level between the upper portion and lower portion of the step is in a range between 40 [to] and 60 micrometers.

18. A method according to claim 15, wherein the conductive bumps are of solder.

19. (Amended) A method for fabricating a semiconductor apparatus according to claim 11, comprising the steps of:

providing a semiconductor wafer on which a plurality of semiconductor devices are formed, each of the semiconductor [device] devices having electrode pads thereon;

forming grooves in the semiconductor wafer at portions corresponding to dicing lines of the semiconductor wafer;

forming an insulating layer on the wafer so that the grooves are filled with the insulating layer but a part of each [the] electrode pad of the semiconductor devices is not covered with the insulating layer;

forming a metal layer on the insulating layer and the part of [the] each electrode [pads] pad, [which is] not covered with the insulating layer;

forming a rewiring layer on the metal layer;

providing a conductive post material [that extend] extending across each of the grooves;

molding the semiconductor wafer with a molding resin so that an upper surface of the molding resin is on the same plane with upper surfaces of the conductive post material across each of the grooves;

providing a conductive bump material on [each of] the conductive post material; and

dicing the semiconductor wafer at the grooves to form a plurality of individual semiconductor [apparatus] apparatuses.

20. A method according to claim 19, further comprising the steps of:

expanding the distance between two adjacent semiconductor devices after the dicing process; and

reflowing the distanced semiconductor devices so as to form a conductive soldering bump on a peripheral side surface of each of the conductive posts.

21. A method according to claim 19, wherein the insulating layer is formed to have a width of 100 to 200μm.

22. A method according to claim 19, wherein the conductive bumps are of solder.

NEW CLAIM

--23. A semiconductor apparatus according to claim 11, wherein the peripheral side surface of each conductive post is formed in the same plane as that of the peripheral side surface of the semiconductor device.--

REMARKS

The Examiner's Action mailed July 3, 2002, has been received and its contents carefully considered. The specification has been amended editorially by